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CONCEPTION OF THE CONTROL CIRCUIT FOR MATRIX CONVERTER WITH SPACE VECTOR MODULATION

This paper deals with control circuit for the Matrix Converter (MC) with space vector modulation (SVM). Hardware and Software proposition for implemented Space Vector control technique are described. Furthermore simulation test results, by means of Matlab simulink, are presented to verify the proposed implementation.

1 INTRODUCTION

In recent years, matrix converters have received considerable attention as a competitor for the commonly used pulse-width modulated voltage-source inverter (PWM-VSI). This is because MC provides voltage and frequency transformation of the three-phase voltage system requiring just a small filter (to get nearly sinusoidal input/output waveforms) which allows for compact design of this circuit. Moreover it provides bi-directional power flow, and a controllable input power factor [1]-[8]. Also falling costs of semiconductors and microprocessors with simultaneous rise of their performance make MC more popular. Although direct SVM techniques have been already introduced [2], [4]-[7], the implementation concepts are continuously developed. Existing implementation and hardware schemas are rather based on Alesina and Venturini [1] or space vector modulation with or without fictitious DC link [3], [2]. Descriptions of the SVM technique implementations are usually superficial and without details. In this paper, implementation concept, general hardware and software description of the control circuit for direct space vector modulation is presented. In section 2 SVM approach based on work [2], developed in works [4]-[6] and presented in [7] is described. Section 3 contains description of Hardware and Software of the proposed control circuit. In section 4 some selected simulation diagrams are shown to confirm functionality of the proposed solution. Conclusions follow in last section.

2 DESCRIPTION OF THE IMPLEMENTED SVM TECHNIQUE

In Fig. 1a) basic scheme of the three-phase MC is shown. Because of commutation lows there are only 27 possible switch configurations (SC). Eighteen active SC described as +1 ÷ -9 and three zero SC described as 0a ÷ 0c (Fig. 1b)), are engaged in

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direct space vector control strategies [2]-[7]. Mathematical model of the MC is described by (1)-(3) [1]-[8].

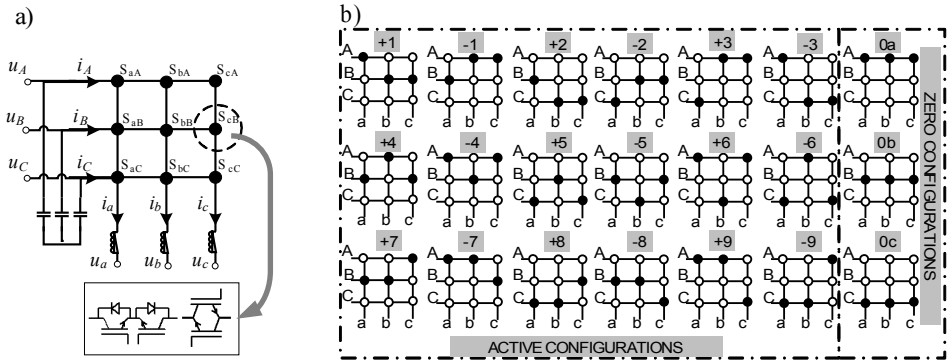

Fig. 1. MC, a) basic scheme, b) active and zero switch configurations.

$$\begin{bmatrix} u_a(t) \\ u_b(t) \\ u_c(t) \end{bmatrix} = \begin{bmatrix} s_{aA}(t) & s_{bA}(t) & s_{cA}(t) \\ s_{aB}(t) & s_{bB}(t) & s_{cB}(t) \\ s_{aC}(t) & s_{bC}(t) & s_{cC}(t) \end{bmatrix} \begin{bmatrix} u_A(t) \\ u_B(t) \\ u_C(t) \end{bmatrix}, \tag{1}$$

$$\mathbf{u_0} = \mathbf{T} \times \mathbf{u_i}, \tag{2}$$

$$\mathbf{i_i} = \mathbf{T}^{\mathbf{T}} \times \mathbf{i_0}, \tag{3}$$

where: $s_{jk} = \begin{cases} 1, \ switch \ S_{jk} \text{ - on} \\ 0, \ switch \ S_{jk} \text{ - off} \end{cases}$, where: $j = \{a,b,c\}, k = \{A,B,C\}$. (4)

The space-vector approach is based on the instantaneous space-vector representation of the input and output voltages and currents. Those representations are created according to transformation (5) [2].

$$\underline{x} = x_1 + x_2 e^{j(2\pi/3)} + x_3 e^{j(4\pi/3)}. \tag{5}$$

The geometrical interpretation of the space vector representations for the line to neutral output voltages and the input line currents, for all active and zero SC (Fig. 1b)) are shown in Fig. 2. Furthermore sector numbers are introduced [7].

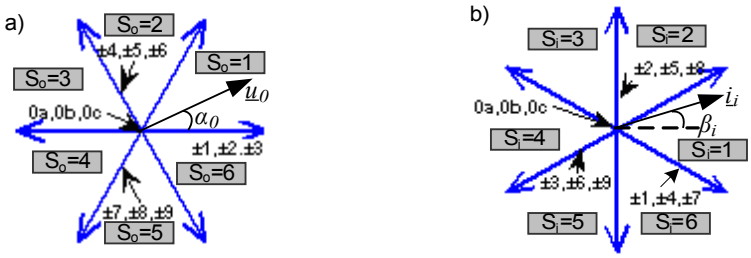

Fig. 2. MC space vector representations for, a) output line-to-neutral voltages, b) input line currents.

$\underline{u}_0 = e^{j\alpha_0}$ *-exemplary line-to-neutral output voltage vector position,* $\underline{i}_i = e^{j\beta_i}$ *- exemplary line input current vector position,* S_o*- sector No. for* $\underline{u}_0$*,* S_i*-sector No. for* $\underline{i}_i$

General description of implemented control strategy is shown on Fig. 3.

Vectors $\underline{i}_i$ and $\underline{u}_0$ are calculated according to (5), sectors $S_{0,}$ $S_{i,}$ (Fig. 2) and phase angles α'_0, β'_i are defined. Those phase angels are defined with respect to the bisecting line of the suitable sector, limited according to (7) and differ then α_0, β_i (Fig. 2, Fig.4) [7].

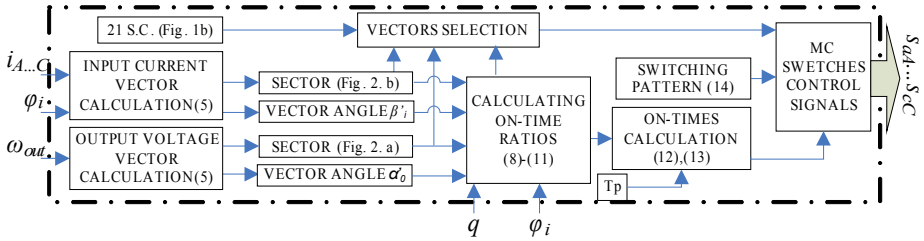

Fig 3. General description of the implemented control strategy
φ_i - input current displacement angle, ω_{out} - output voltage pulsation, q - voltage transfer ratio, T_p - time period.

$$-\pi/6 < \alpha'_0 < \pi/6, \qquad -\pi/6 < \beta'_i < \pi/6 \tag{7}$$

On-time ratios are expressed as follows [7]:

$$\delta_1 = (-1)^{S_0+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0-\pi/3)\cos(\beta'_i-\pi/3)}{\cos\varphi_i}, \tag{8}$$

$$\delta_2 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0-\pi/3)\cos(\beta'_i+\pi/3)}{\cos\varphi_i}, \tag{9}$$

$$\delta_3 = (-1)^{S_0+S_i}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0+\pi/3)\cos(\beta'_i-\pi/3)}{\cos\varphi_i}, \tag{10}$$

$$\delta_4 = (-1)^{S_0+S_i+1}\frac{2}{\sqrt{3}}q\frac{\cos(\alpha'_0+\pi/3)\cos(\beta'_i+\pi/3)}{\cos\varphi_i}. \tag{11}$$

Four active and one zero SC are selected based on knowledge about actual sectors and signs of the on-time ratios according to Tab. 2 and Tab. 3. Positive on-time ratio means that the positive SC has to be selected and negative ratio requires a negative SC [7].

Tab. 1. Selection of the active SC for each combination of So and Si

		Sector of the output voltage vector $\underline{u}_o$ (So)											
		1 or 4				**2 or 5**				**3 or 6**			
$\underline{i}_i$ (Si)Sector of the	**1 or 4**	±9	±7	±3	±1	±6	±4	±9	±7	±3	±1	±6	±4
	2 or 5	±8	±9	±2	±3	±5	±6	±8	±9	±2	±3	±5	±6
	3 or 6	±7	±8	±1	±2	±4	±5	±7	±8	±1	±2	±4	±5
		δ_1	**δ_2**	**δ_3**	**δ_4**	**δ_1**	**δ_2**	**δ_3**	**δ_4**	**δ_1**	**δ_2**	**δ_3**	**δ_4**

Tab. 2. Selection of the zero SC for each combination of So and Si

		Sector for $\underline{u}_o$ (So)					
		1 or 4		**2 or 5**		**3 or 6**	
Sector $\underline{i}_i$ (Si)	**1 or 4**	0_B	0_A	0_B	0_A	0_B	0_A
	2 or 5	0_A	0_C	0_A	0_C	0_A	0_C
	3 or 6	0_C	0_B	0_C	0_B	0_C	0_B
		$\boldsymbol{\delta_4}$	$\boldsymbol{-\delta_4}$	$\boldsymbol{\delta_4}$	$\boldsymbol{-\delta_4}$	$\boldsymbol{\delta_4}$	$\boldsymbol{-\delta_4}$

Output voltage $\underline{u}_o$ and input current $\underline{i}_i$ vectors are created as shown in Fig. 4.Vector $\underline{u}_0$ is set up of two components $\underline{u}'_0$ and $\underline{u}''_0$, which are created by switching on four earlier selected vectors (+3, -9, +7, -1) through suitable times during the cycle period. Furthermore in Fig. 4b) it is shown how the control of φ_i is achieved by controlling βi. Switched-on times for vectors are calculated from (8), (9), (10), (11) and expressed by (12), (13). Vector switching order during the cycle period can be considered according to (14) [7]. For example $\frac{1}{2}\delta_3$ means that the vector assigned in Tab. 2 for symbol δ_3 and selected according to all rules given above should be switched on first for the time $\frac{1}{2}|\delta_3| T_p$.

$$t_1 = |\delta_1| * T_p; \quad t_2 = |\delta_2| * T_p; \quad t_3 = |\delta_3| * T_p; \quad t_4 = |\delta_4| * T_p \tag{12}$$

$$t_0 = |\delta_0| T_p = (|\delta_1| + |\delta_2| + |\delta_3| + |\delta_4|) T_p - T_p \tag{13}$$

$$\frac{1}{2}\delta_3 \rightarrow \frac{1}{2}\delta_1 \rightarrow \frac{1}{2}\delta_2 \rightarrow \frac{1}{2}\delta_4 \rightarrow \delta_0 \rightarrow \frac{1}{2}\delta_4 \rightarrow \frac{1}{2}\delta_2 \rightarrow \frac{1}{2}\delta_1 \rightarrow \frac{1}{2}\delta_3 \tag{14}$$

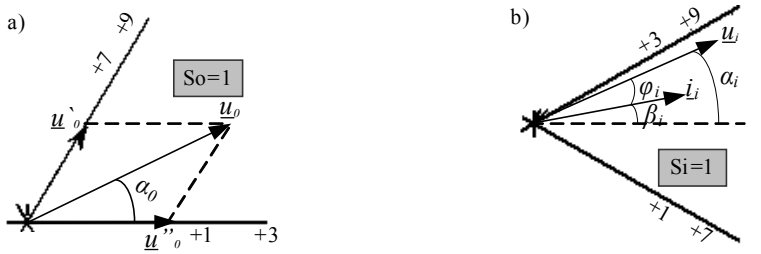

Fig. 4.Vector modulation description, a) for exemplary output voltage vector position, b) for exemplary input current vector position.

3 CONCEPTION OF CONTROL CIRCUIT FOR MC

Discussed SVM is complicated and demands advanced hardware solution. In a real control circuit it is also necessary to apply one of the commutation strategies with or without "dead times" which makes a control program more complicated. Proposed hardware solution consists of two DSP (P0, P1) processors (ADSP21836), RAM (Dual port. SRAM 1Mb), FLASH (512kx8) [11] and one FPGA (XC3S200), (Fig. 5a, Tab. 3).

First DSP (P0) (Fig. 5) acquires measured samples of input voltages and output currents via ADCs. Because of input current distortion, it is easier to find $\underline{i}_i$ on the basis of input voltage values taking into account φ_i as shown in Fig. 4b.

Table 3. ADSP 21368 and FPGA XC3S200 data specification.

ADSP21836			
Manufactured by:	Analog Devices	On-Chip ROM	6 MBit
Clock Speed	400 MHz	Divide time (y/x)	7.5 ns

Instruction Cycle Time	2.5 ns	Mult. time:[3x3]*[3x1]	11.25 ns
MFLOPS Sustained	1600 MFLOPS	Programmed via	JTAG
On-Chip SRAM	2 Mbit	Development Soft.	VisualDSP 5.0++
XC3S200			
Manufactured by:	Xilinx	Block RAM Bits	216k
System Gates	200000	Programmed via	JTAG
Max Differential I/0Pairs	76	Development Soft.	WebPACK

Five selected vectors and calculated by P0 absolute values of (2), (3), (4), (5) are the input signals for second processor (P1). P1 displays nine signals ($s_{aA} \div s_{cC}$) according to selected SC and chosen switching pattern during the proper times.

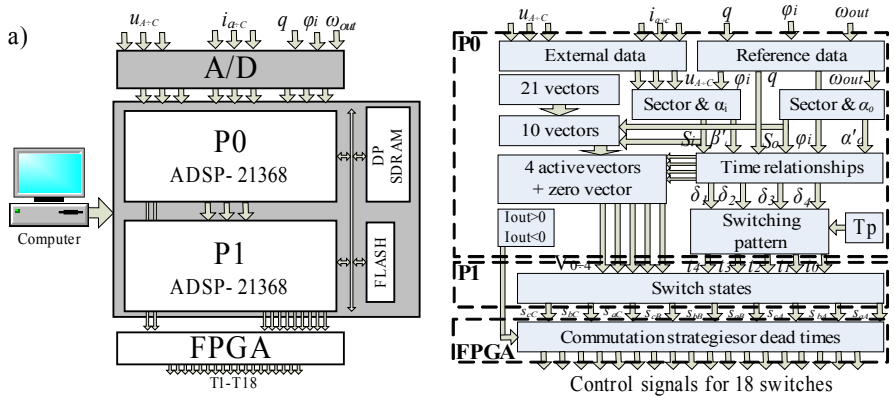

Fig. 5.Hardware of the control circuit a) block scheme, b) functional scheme

Implemented double side switching pattern (8) can be achieved as illustrated in Fig.6, where values of (15) are compared to saw waveform giving local duty times d_0-d_4 for selected vectors during the cycle period T_p.

$$d_1 = |\delta_3|; \quad d_2 = |\delta_3| + |\delta_1|; \quad d_3 = |\delta_3| + |\delta_1| + |\delta_2|; \quad d_4 = |\delta_3| + |\delta_1| + |\delta_2| + |\delta_4|; \qquad (15)$$

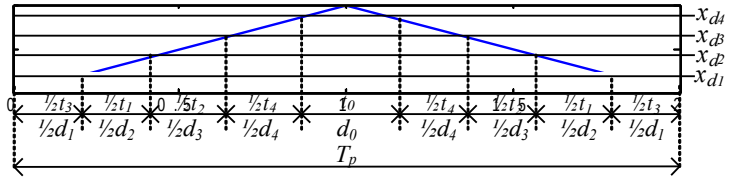

Fig. 6. Exemplary switching pattern description.

Nine output signals from P1 ($s_{aA} \div s_{cC}$) are converted, by means of FPGA, in to 18 control signals for MC transistors. In FPGA commutation strategy is also realized. Following software tools for discussed control strategy are used: VisualDSP 5.0++ dedicated to programming ADSP-21836 includes debugger, C/C++ compiler, assembler, linker, and simulator [9]. WebPACK dedicated for programming FPGA and CPLD, offers HDL synthesis, simulation, implementation and device fitting [10]. Nine switching states ($s_{aA} \div s_{cC}$) obtained in Matlab simulation (section 4) are send to memory of P1 and then P1 output signals are converted by FPGA.

4 SIMULATION TEST RESULTS

Exemplary time waveforms for discussed MC (Fig. 1a, Fig. 3) obtained by Matlab simulink are shown in Fig. 7. Simulation test parameters are collected in Tab. 4.

Table 3. Simulation parameters

Supply	3x400 V/ 50 Hz	Sequence period, T_p	0.4 ms
Input filter L / C	0.5 mH / 30 μF	Load R / L	10 Ω / 0.5 mH

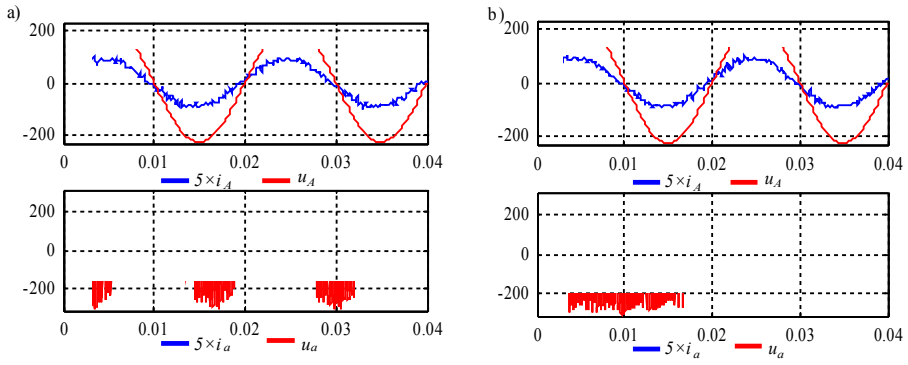

Fig .7. Voltage and current time waveforms in MC main circuit for q=0.866, φ_i=0°, a) fout=75 Hz, b) fout=25 Hz.

5 CONCLUSIONS

In this paper the concept of the control circuit of MC with implemented space vector modulation has been presented. Simulation results have confirmed that the presented control technique exploits the MC's possibility to control the input power factor regardless the output power factor, reducing switching commutations per cycle period and using input voltages fully. In presented concept simulation test results are utilized in proposed control circuit. Total SVM control strategy implementation in the proposed hardware solution will be the subject of investigation in the near future.

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